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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,091	01/02/2004	Brian H. Moeckly	10467.43USI2	2150

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EXAMINER	
WARTALOWICZ, PAUL A	

ART UNIT	PAPER NUMBER
1793	

MAIL DATE	DELIVERY MODE
10/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,091	MOECKLY ET AL.	
	Examiner	Art Unit	
	Paul A. Wartalowicz	1793	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) *22-58* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/9/07, 5/23/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 7/9/07 have been fully considered but they are not persuasive.

Applicant states that the traversal is that Applicant does not necessarily agree with or wish to be bound by Examiner's rationale in proposing the request for restriction of examination.

Therefore, the restriction is deemed FINAL.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in view of Chan (U.S. 5,892,243).

Figure 2 of Harada et al. shows a Josephson junction having a crystalline substrate MgO, a YBCO electrode formed on and epitaxial to the substrate (page 1389, column 1, lines 4-7), an insulator a-YSZ, a barrier comprising a plasma-treated surface of the YBCO (page 1387, column 1, second paragraph), and a YBCO counter-electrode formed directly on and epitaxial to the barrier. Chan teaches with respect to the cover

figure to form insulator 48 epitaxially on YBCO 46 (column 6, lines 25-32). It would have been obvious to form an epitaxial insulator on the Harada device instead of a-YSZ, in order to obtain the higher quality crystalline material obtained by epitaxial growth.

With respect to claims 2-4, a process limitation carries weight in a claim drawn to a product only when distinct structure is produced by the process. *In re Thorpe*, 227 USPQ 964 (Fed. Cir. 1985). There is no evidence of record to show that the process steps recited would necessarily give rise to a barrier layer distinct from that of Harada et al. With respect to claim 5, both of the Harada YBCO layers have their c-axis perpendicular to the substrate (page 1389, column 1, lines 4-7). So the top plane of the lower YBCO must be an a-b plane, and a junction is formed in that plane.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in view of Chan (U.S. 5,892,243) and Laibowitz et al. ("All high T_c edge junctions and SQUIDS").

Laibowitz et al. teaches at the bottom of column 1 of page 686 that transport along the a-b plane direction has a longer coherence length and higher current density. It would have been obvious to arrange a junction perpendicular to the a-b plane for these reasons. The device of Harada figure 2 has a perpendicular portion of the junction that would be perpendicular to the a-b plane, because the c direction is perpendicular to the MgO substrate.

Claims 8-12, 14-19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in view of Chan (U.S. 5,892,243) and any one of Hunt et al. ("High Temperature Superconductor Josephson Weak Links") or Ishimaru et al. ("Evaluation of fabrication process and barrier structure for interface-modified ramp-edge junctions") or Kito et al. ("Excess-current-free stacked Josephson junctions with high I_cR_n product") or Moeckly et al. ("Interface-Engineered High-T_c Josephson Junctions").

Harada et al. fail to teach the claimed I_cR_n product.

However, Hunt et al. teach that it is known for YBCO with microbridges to exhibit an I_cR_n product of around 1.03 mV at a temperature of 4.2 K and an I_cR_n product of around 450 μV a temperature of 77 K (pg 4). Ishimaru et al. teach YBCO junctions (pg 1327) wherein the I_cR_n product is around 1.00-3.00 mV at a temperature of 4.2 K (pg 1330). Kito et al. teach YBCO junctions (pg 1326) wherein the I_cR_n product is around 2.02 mV at a temperature of 4.2 K (pg 1323-24). Moeckly et al. teach YBCO junctions (pg 2) wherein the I_cR_n product is around 1.00-3.00 mV at a temperature of 4.2-40 K (pg 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time applicant's invention was made to provide the claimed I_cR_n product in Harada et al. because the fabrication method for making YBCO devices exhibiting the claimed I_cR_n product are known as taught by any one of Hunt et al. (pg 4), Ishimaru et al. (pg 1330), Kito et al. (pg 1323-24), and Moeckly et al. (pg 6).

Claims 8-12, 14-19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in view of Chan (U.S. 5,892,243) and Satoh et al. ("Effect of Lanthanum Doping of YbaCuO...").

Harada et al. fail to teach the claimed I_cR_n product.

Satoh et al., however, teach a method of making YBCO (pg 1) wherein lanthanum doped YBCO produces a higher I_cR_n product than that of pure YBCO (pg 2, 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time applicant's invention was made to provide a higher I_cR_n product than that of pure YBCO (pg 2, 3) in Harada et al. because it is known to dope YBCO with lanthanum in order to obtain high I_cR_n product.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize an I_cR_n product, since it has been held that discovering an optimum value or a result effective variable involved only routine skill in the art. In re Boesch, 617 F.2nd 272, 205 USPQ 215 (CCPA 1980). The artisan would have been motivated to optimize an I_cR_n product by the reasoned explanation that higher I_cR_n product enables annealing at higher temperatures for longer durations (pg. 3) as taught by Satoh et al.

Claims 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in view of Chan (U.S. 5,892,243) and Laibowitz et al. ("All high T_c edge junctions and SQUIDS") and any one of Hunt et al. ("High Temperature Superconductor Josephson Weak Links") or Ishimaru et al. ("Evaluation of fabrication process and barrier structure for interface-modified ramp-edge junctions") or Kito et al. ("Excess-current-free stacked Josephson junctions with high I_cR_n product") or Moeckly et al. ("Interface-Engineered High-T_c Josephson Junctions").

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Wartalowicz whose telephone number is (571) 272-5957. The examiner can normally be reached on 8:30-6 M-Th and 8:30-5 on Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stanley Silverman can be reached on (571) 272-1358. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Wartalowicz
September 18, 2007

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